FSB-1611

High Performance

- Socket 370/Pentium III
- 133MHz FSB, VGA, LAN, WDT, DOC

Industrial PC Products User's Manual

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CHAPTER 1 INTRODUCTION

This user's manual is for FSB-1611 CPU card, which is designed by expert colony. It is based on 815E, please refer to the corresponding contents according to the product you purchased.

This chapter provides you information on the FSB-1611 CPU card. It is divided into the following sections:

- **Description**
- **Specifications**
- **Layout**

Description

The 1611 is a PGA370 package Industrial CPU Card based on Intel's 815E B-step and ICH2 chipset and is fully designed for harsh industrial environment. It features a Socket-370 processor connector. And it integrated onboard VGA and 2/1/0 Intel 82559/ER Base-T 10/100MHz Ethernet controllers.

Specifications

System Architecture

- 815E IPC
- Intel Celeron^{TM}II/Pentium III with 66/100/133MHz FSB
- PCI V2.1 compliant
- 5.0V tolerant PCI and ISA interface

CPU Supported

- Support 66/100/133MHz system bus
- Support Intel Pentium Tualatin FC-PGA2 1.13/1.20/1.26GHz （133MHz ）or higher
- Support Intel Pentium (Coppermine) FC-PGA 533/600/667/733/800/866/933M/ 1GHz (133MHz)
- Support Intel Pentium (Coppermine) FC-PGA 500/550/600/650/700/750/800 /850M/ 1G/1.1GHz (100MHz)
- Support Intel Celeron FC-PGA 533/566/600/633/667/700/733MHz (66MHz)
- Support Intel Celeron FC-PGA 1GHz or higher (100MHz)

Chipset
- Intel 815E B-Step +ICH2 Chipset
- 100/133MHz FSB supported
- PCI V2.1 compliant
- Optimized SDRAM supported

Main Memory
- Support Dual DIMM up to 512MB (Max.)

BIOS
- Award PCI BIOS
- Plug & Play supported
- Advanced Power Management supported
- Temperature/Voltage check
- Over 80 Temperature Shutdown (Operations can be set using BIOS)
- 2M/4M bit flash ROM
- Hot swap supported
- Support Watchdog (system rest) Operations can be set using BIOS
- Support DOC2000

VGA
- Integrated graphics acceleration controller that support 3D/2D enhancements

On Board LAN (Optional)
- 2/1/0 Intel 82559/ER 10/100 Base -T Ethernet controllers (please refer to section 3.3)
- Support full duplex
- Compliant with PCI V2.1, IEEE802.3, IEEE802.3U
- Driver supported: DOS /Windows, Windows 98/2000, Windows NT4.0 or Linux

On Board I/O
- Winbond W83627 LPC controller
- Bi-directional PIO port, support EPP/ECP
- Built-in FDC support 3.5" 720K/1.44MB/(Rear I/O only)
- On chip keyboard/ mouse controller, 6 pin mini DIN for both PS /2 mouse and keyboard (Front I/O & Rear I/O)
- On board buzzer
- On board IrDA Connector
- Dual IDE (Support UltraDMA/33/66/100MB/Sec)
- Dual USB1.1 ports

On Board RTC
- High precision real time clock/calendar with battery backup

On Board DOC2000
- On board reserved socket for DOC2000

System Monitor
- Winbond W83627HF system monitor controller
- System voltage (Vcore, +3.3v, +5v, +12v, Vtt)
- Fan speed (For CPU)
- Two temperature controllers (for CPU and for system)

Watchdog Timer (software)
- 1,2,4…64 seconds time-out intervals
- Operations can be set using BIOS
- Maximum timeout interval: 64 seconds

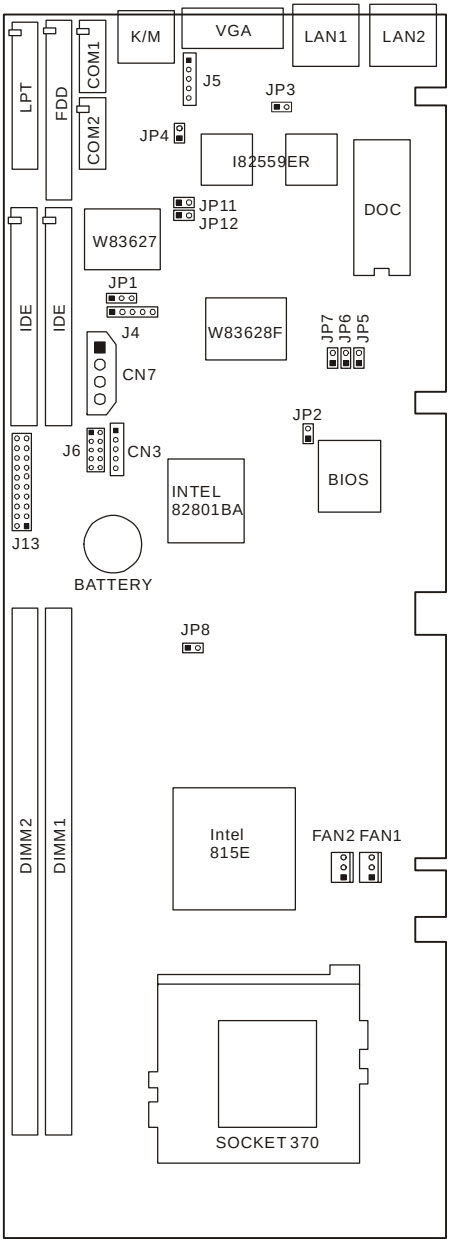
Dimensions
- IPC size based, 338mm (L) x 122 mm (W)

Power Requirements
- +5V, 10A(Max.)
- +12V, 3A (Max.)

Environments
- Operating temperatures: 0˚C to 60˚C
- Storage temperatures: -20˚C to 80˚C
- Relative humidity: 10% to 90% (Non-condensing)

Operating system support
- Windows 98/Windows 2000/Windows NT 4.0, Linux

Layout



■ The square represent Pin 1 of the jumpers/connectors

CHAPTER 2 INSTALLATIONS

This chapter provides information on how to use the jumpers and connectors on the FSB-1611 in order to set up a workable system.

2.1 CPU Installation

The FSB-1611 Industrial CPU Card supports a Socket-370 connector processor socket for PGA370 Package processors. To install the processor, unlock the mechanism of the socket, push the processor into the socket with right access, and then lock the mechanism of the socket. After doing this, secure the CPU FAN on the socket. This design allows easy installation of the CPU and higher integration for more I/O space. To uninstall the Socket-370 processor, simply push the locking mechanism on the socket and remove the Socket-370 processor. No tool is needed.

2.2 Memory Installation

The FSB-1611 Industrial CPU Card supports two 168-pin DIMM sockets for a maximum total memory of 512MB SDRAM.

In populating the DIMM sockets, DIMM1 or DIMM2 bank should be populated first. Refer to the following table on how to configure the memory.

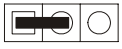
168-pin DIMM (3.3V) SDRAM board

Bank0 (DIMM2)	Bank1 (DIMM1)	Total Memory
8MB	-----	8MB
16MB	-----	16MB
32MB	-----	32MB
64MB	-----	64MB
128MB	-----	128MB
8MB	8MB	16MB
16MB	8MB	24MB
32MB	8MB	40MB
64MB	8MB	72MB
128MB	8MB	136MB
16MB	16MB	32MB
32MB	16MB	48MB
64MB	16MB	80MB
128MB	16MB	144MB
32MB	32MB	64MB
64MB	32MB	96MB
128MB	32MB	160MB
64MB	64MB	128MB
128MB	64MB	192MB
128MB	128MB	256MB
256MB	256MB	512MB

CHAPTER 3 JUMPER SETTINGS

The jumpers on the FSB-1611 allow you to configure your CPU card according to the needs of your applications. If you have doubts about the best jumper configuration for your needs, contact your dealer or sales representative.

3.1 Jumper Presentation



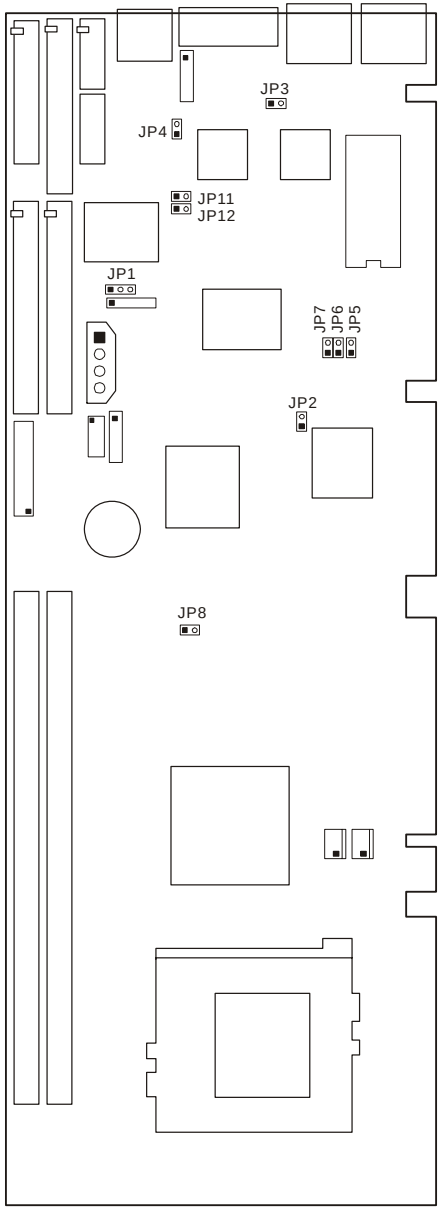
Pins 1 and 2 are shorted with a jumper cap.

Pins 2 and 3 are shorted with a jumper cap.

The jumper is shorted when the jumper cap is placed over the two pins of the jumper.

The jumper is opened when the jumper cap is removed from jumper.

3.2 Jumper location of FSB-1611



■ The square represent Pin 1 of the jumpers/connectors

3.3 Jumper Settings

Function		Settings
Clear CMOS Data	Normal	JP1: 1-2
	Clear	JP1: 2-3
BIOS Setting	Unlocked	JP2: Open
	Locked	JP2: Short
LAN 2 Setting	Enabled	JP3: Short
	Disabled	JP3: Open
LAN 1 Setting	Enabled	JP4: Short
	Disabled	JP4: Open
DOC Address Settings	D000H	JP5: Short
	D800H **(Default)**	JP6: Short
	C800H	JP7: Short
CPU Selection	Auto detect **(Default)**	JP8: Open
	Tualatin Celeron 1GHz CPU (100MHz FSB)	JP8: Short
COM2 Port Setting	232	JP11: Open JP12: Short
	422/485	JP11: Short JP12: Open

LAN Port Settings

The mainboard can supply up to 2 RJ-45 LAN ports, please configure depends on your requirement.

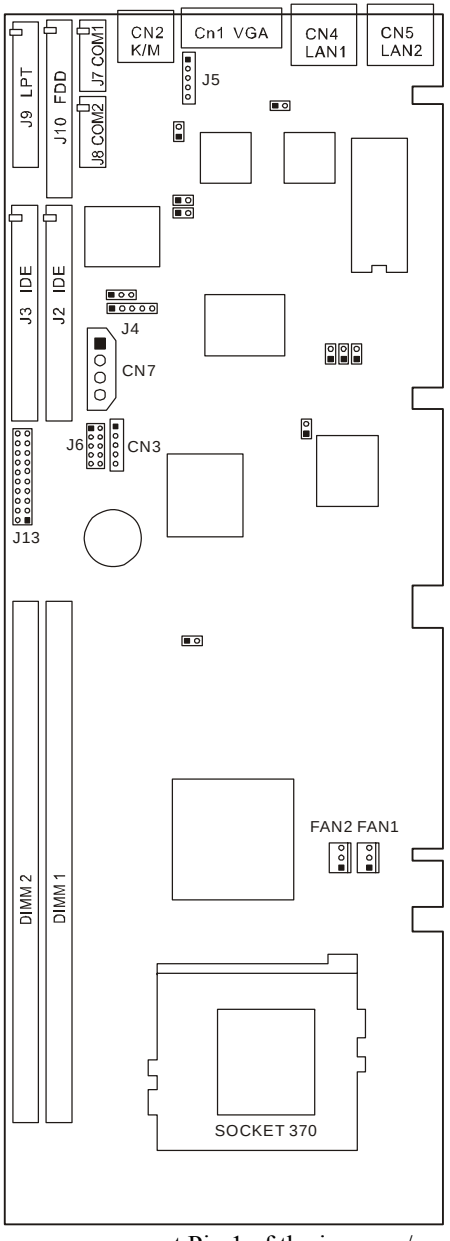
LAN port amount	Jumper Settings
2	JP4 short; JP3 short
1	JP4 short; JP3 open
0	JP4 open; JP3 open

CHAPTER 4 CONNECTOR CONFIGURATION

The connectors on the FSB-1611 are used to connect external devices such as keyboard, floppy disk drives, hard disk drives, printers, etc. The following table lists the connectors on FSB-1611 and their respective functions.

Location	Function
J2/J3	IDE Connectors
J4	IrDA Connector
J5	External Keyboard connector
J6	USB connector
J7	COM1 Port Connector
J8	COM2 Port Connector
J9	Parallel Port Connector
J10	Floppy Drive Connector
J13	System Panel Connector
FAN1/2	Fan Power Connector
CN1	VGA Connector
CN2	Keyboard/Mouse Connector
CN3	External ATX Power Connector
CN4/5	LAN Connector
CN7	Power Connector

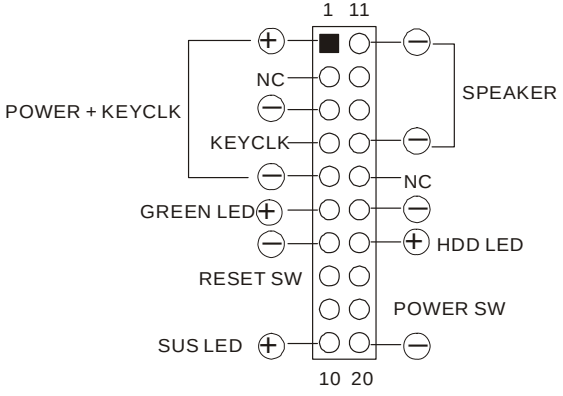
Connector Location



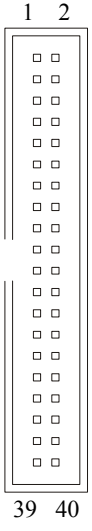
■ The square represent Pin 1 of the jumpers/connectors

4.1 System Panel Connector

J13 is a 20-pin system panel multi-function connector. The pin assignments is as below:



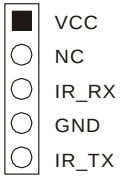
4.2 IDE Connectors



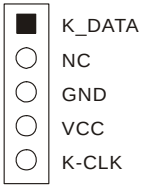
Signal Name	Pin #	Pin #	Signal Name
Reset IDE	1	2	Ground
Host data 7	3	4	Host data 8
Host data 6	5	6	Host data 9
Host data 5	7	8	Host data 10
Host data 4	9	10	Host data 11
Host data 3	11	12	Host data 12
Host data 2	13	14	Host data 13
Host data 1	15	16	Host data 14
Host data 0	17	18	Host data 15
Ground	19	20	Key
DRQ0	21	22	Ground
Host IOW	23	24	Ground
Host IOR	25	26	Ground
IOCHRDY	27	28	Host ALE
DACK0	29	30	Ground
IRQ14	31	32	No connect
Address 1	33	34	No connect
Address 0	35	36	Address 2
Chip select 0	37	38	Chip select 1
Activity	39	40	Ground

4.3 IrDA Connector

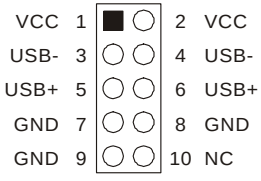
J4 is used for an IrDA connector for wireless communication.



4.4 J5 - External Keyboard Connector

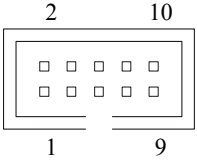


4.5 J6 - USB Connector



4.6 COM Serial Port

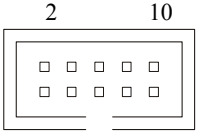
J7 is a 10-pin header connector, which is the onboard COM1 serial port of the FSB-1611. The following table shows its pin assignments.



COM1

Pin #	Signal Name
1	DCD, Data carrier detect
3	RXD, Receive data
5	TXD, Transmit data
7	DTR, Data terminal ready
9	GND, ground
2	DSR, Data set ready
4	RTS, Request to send
6	CTS, Clear to send
8	RI, Ring indicator
10	GND, ground

J8 is a 10-pin header connector, which is the onboard COM2 serial port of the FSB-1611. The following table shows its pin assignments.



COM1

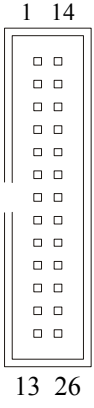
Pin #	Signal Name		
	RS-232	**RS-422**	**RS-485**
1	DCD	TX-	DATA-
3	RX	TX+	DATA+
5	TX	RX+	NC
7	DTR	RX-	NC
9	GND	GND	GND
2	DSR	RTS-	NC
4	RTS	RTS+	NC
6	CTS	CTS+	NC
8	RI	CTS-	NC
10	GND	GND	GND

COM2 Port Setting

232	JP11: Open JP12: Short
422/485	JP11: Short JP12: Open

4.7 Parallel Port Connector

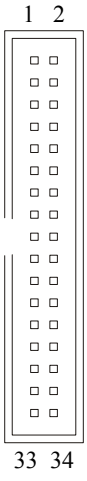
The following table describes the pin assignments of this connector.



Signal Name	Pin #	Pin #	Signal Name
Line printer strobe	1	14	AutoFeed
PD0, parallel data 0	2	15	Error
PD1, parallel data 1	3	16	Initialize
PD2, parallel data 2	4	17	Select
PD3, parallel data 3	5	18	Ground
PD4, parallel data 4	6	19	Ground
PD5, parallel data 5	7	20	Ground
PD6, parallel data 6	8	21	Ground
PD7, parallel data 7	9	22	Ground
ACK, acknowledge	10	23	Ground
Busy	11	24	Ground
Paper empty	12	25	Ground
Select	13	N/A	N/A

4.8 Floppy Drive Connector

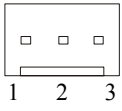
J10 is a 34-pin header and will support up to 2.88MB floppy drives.



Signal Name	Pin #	Pin #	Signal Name
Ground	1	2	RM/LC
Ground	3	4	No connect
Ground	5	6	No connect
Ground	7	8	Index
Ground	9	10	Motor enable 0
Ground	11	12	Drive select 1
Ground	13	14	Drive select 0
Ground	15	16	Motor enable 1
Ground	17	18	Direction
Ground	19	20	Step
Ground	21	22	Write data
Ground	23	24	Write gate
Ground	25	26	Track 00
Ground	27	28	Write protect
Ground	29	30	Read data
Ground	31	32	Side 1 select
Ground	33	34	Diskette change

4.9 Fan Power Connector

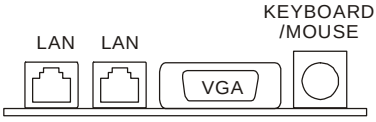
FAN1 and FAN2 are 3-pin headers for the CPU or system fan. The fan must be a 12V fan.



Pin #	Signal Name
1	Ground
2	+12V
3	Rotation

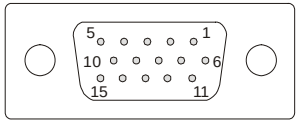
4.10 Rear Panel Connectors

The connectors on rear panel include two RJ-45 LAN ports, one VGA port, and the PS/2 mouse/keyboard port.



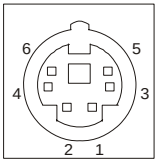
CN1: VGA CRT Connector

The pin assignments of VGA CRT connector are as follows:



Signal Name	Pin	Pin	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
N.C.	9	10	GND
N.C.	11	12	SDATA
HSYNC	13	14	VSYNC
SCLK	15		

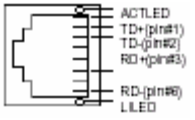
CN2 - PS/2 Keyboard/Mouse Connector



Pin #	Signal Name
1	Keyboard data
2	Mouse data
3	GND
4	5V
5	Keyboard clk
6	Mouse clk

RJ-45 Connector

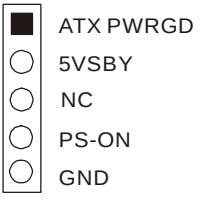
CN4/CN5 are for the 10/100Mbps Ethernet capability of the CPU card. The figure below shows the pin assignments of this connector and its corresponding input jack. LILED and ACTLED are green and yellow LED indicators located at both side of the RJ45 connector that shows LAN activity and the transfer rate in progress. Refer to the following table for the functions of each LED status.



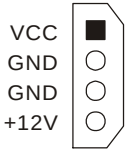
LILED (green) Status	Function	ACTLED (yellow) Status	Function
ON	Valid link	OFF	Data transfer in progress
OFF	Invalid link or Link off	ON	Data transfer off

4.11 ATX Power Supply Connectors

CN3 - External ATX Power Connector



CN7 –Power Connector



CHAPTER 5 AWARD BIOS UTILITY

This chapter describes the different settings available in the Award BIOS that comes with the FSB-1611 CPU card.

5.1 Entering Setup

Power on the computer, when the following message briefly appears at the bottom of the screen during the POST (Power On Self Test), press <Del> key or simultaneously press the <Ctrl> + <Alt> + <Esc> keys, to enter the AWARD BIOS CMOS Setup Utility.

Press <Del> to enter SETUP

Once you have entered, the Main Menu appears on the screen. The main menu allows you to select from eleven setup functions and two exit choices.

Use the arrow keys to select the item and press <Enter> to accept or enter the sub-menu.

CMOS Setup Utility – Copyright (C) 1984 – 2001 Award Software	
►Standard CMOS Features	►Frequency/Voltage Control
►Advanced BIOS Features	Load Fail – Safe Defaults
►Advanced Chipset Features	Load Optimized Defaults
►Integrated Peripherals	Set Supervisor Password
►Power Management Setup	Set User Password
►PnP/PCI Configurations	Save & Exit Setup
►PC Health Status	Exit Without Saving
Esc: Quit F9: Menu in BIOS F10: Save & Exit Setup	↑↓→←: Select Item
Load Optimized Defaults	

5.2 Standard CMOS Features Setup

The basic CMOS settings included in "Standard CMOS Features" are Date, Time, Hard Disk Drive Types, Floppy Disk Drive Types, and VGA etc. Use the arrow keys to highlight the item, and then use the <PgUp> or <PgDn> keys to select the value desired in each item.

CMOS Setup Utility – Copyright (C) 1984- 2001 Award Software Standard CMOS Features		
Date (mm:dd:yy) Time (hh:mm:ss)	Sat. Jun 16 2001 11:23:33	Item Help
►IDE Primary Master ►IDE Primary Slave ►IDE Secondary Master ►IDE Secondary Slave		Menu Level ►
Drive A Drive B	[1.44M, 3.5 in.] [None]	Change the day, month, year and century
Video Hal On	[EGA/VGA] [All, But Keyboard]	
Base Memory Extended Memory Total Memory	640K 63488K 64512K	
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10: Save ESC: Exit F1:General Help F5: Previous Values F6: Fail - Save Defaults F7: Optimized Defaults		

Date/Time
Set the system date and time.

IDE Primary/Secondary Master/Slave
The BIOS will automatically detect the IDE drives' type.

Drive A/B
Set the type of floppy drives installed.

Video
Set the type of video display card installed in your system.
Options:
EGA/ VGA: For EGA, VGA, SEGA, SVGA, or PGA monitors adapters.
CGA 40: Color Graphic Adapter, powering up in 40-column mode.
CGA 80: Color Graphic Adapter, powering up in 80-column mode.
MONO: Monochrome adapter, including high-resolution monochrome adapters.

Halt On
This field determines whether the system will stop if an error is detected during powering up.
Options:
No errors: The system boot will not stop for any error that may be detected.
All errors: Stop and prompt whenever the BIOS detect a non-fatal error.
All, But Keyboard: Stop and prompt for all other errors but a keyboard error.
All, But Diskette: Stop and prompt for all other errors but a diskette error.
All, But Disk/Key: Stop and prompt for all other errors but a keyboard or disk error.

Memory
This is a Display-Only Category, determined by POST of the BIOS.
Base Memory: The amount of base (or conventional) memory installed in the system.
Extended Memory: How much extended memory is presented during the POST.
Total Memory: The sum of the above memory.

5.3 Advanced BIOS Features Setup

CMOS Setup Utility – Copyright (C) 1984 – 2001 Award Software Advanced BIOS Features		
Virus Warning	[Disabled]	Item Help
CPU Internal Cache	[Enabled]	
External Cache	[Enabled]	Menu Level ►
CPU L2 Cache ECC Checking	[Enabled]	
Processor Number Feature	[Enabled]	Allows you to choose the VIRUS warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area. BIOS will show a warning message on screen and alarm beep
Quick Power On Self Test	[Enabled]	
First Boot Device	[Floppy]	
Second Boot Device	[HDD – 0]	
Third Boot Device	[LS120]	
Boot Other Device	[Enabled]	
Swap Floppy Drive	[Disabled]	
Boot Up Floppy Seek	[Enabled]	
Boot Up Numlock Status	[On]	
Gate A20 Option	[Fast]	
Security Option	[Setup]	
OS Select For DRAM > 64MB	[Non – OS2]	
Report No FDD For Win95	[No]	
Video BIOS Shadow	[Enabled]	
C8000-CBFFF Shadow	[Disabled]	
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10: Save ESC: Exit F1:General Help F5: Previous Values F6: Fail - Save Defaults F7: Optimized Defaults		

Virus warning
When enabled, guards against boot virus threats early in the On Guard boot cycle, before they have a chance to load into your system, ensuring your computer boots to a clean operating system.

CPU Internal Cache
Enabled speeds up memory access. However, it depends on CPU/chipset design.

External Cache
Enables external L2 cache allows better performance.

CPU L2 Cache ECC Checking
Enabled will enables CPU L2 Cache ECC function.

Processor Number Feature
When Pentium III CPU is installed, choose *Enabled* to make the serial number readable.

Quick Power On Self Test
Enabled allows skip some tests during POST. *Disabled* is Normal POST.

First/Second/Third/Other Boot Device
Select Your Boot Device Priority. It could be Floppy, LS120, HDD-0, SCSI, CDROM, HDD-1, HDD-2, HDD-3, ZIP100, and LAN.

Swap Floppy Drive
If the system has two floppy drives, choose enabled to assign physical drive B to logical drive A and vice-versa.

Boot Up Floppy Seek
Tests the tracks of floppy drive to determine whether they have 40 or 80 tracks.

Boot Up NumLock Status
On/ Off: Selects power on state for NumLock.

Gate A20 Option
Normal/ Fast: Lets chipset control GateA20, or Normal - a pin in the keyboard controller controls GateA20. Default is Fast.

Security Option
Setup/ System: Determine whether the password is required every time the system boots or only when you enter setup.

OS Select For DRAM>64MB
Non-OS2/ OS2: Selects OS2 only if you are running OS/2 operating system with more than 64MB of RAM.

Report NO FDD for WIN 95
Yes/ No: Choose Yes to report NO Floppy Disk Drive for WIN 95 to release IRQ6.

Video BIOS Shadow
Allow you to change the Video BIOS location from ROM to RAM. Video Shadow will increase the video speed.

C8000-CBFFF Shadow / DC000-DFFFF Shadow
Shadowing a ROM reduces the memory available between 640KB to 1024KB. These fields determine whether or not optional ROM will be copied to RAM.

5.4 Advanced Chipset Features Setup

CMOS Setup Utility – Copyright (C) 1984 – 2001 Award Software Advanced Chipset Features		
SDRAM CAS Latency Time	[Auto]	Item Help
SDRAM Cycle Time Tras/Trc	[Auto]	
SDRAM RAS – to – CAS Delay	[Auto]	Menu Level ►
SDRAM RAS Precharge Time	[Auto]	
System BIOS Cacheable	[Disabled]	
Video BIOS Cacheable	[Disabled]	
Memory Hole At 15M – 16M	[Disabled]	
CPU Latency Timer	[Enabled]	
Delayed Transaction	[Enabled]	
AGP Graphics Aperture Size	[64MB]	
System Memory Frequency	[Auto]	
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10: Save ESC: Exit F1:General Help F5: Previous Values F6: Fail - Save Defaults F7: Optimized Defaults		

SDRAM CAS Latency Time
Auto 2/ 3: Contains the information for SDRAM initialization procedure.

SDRAM Cycle Time Tras/Trc :
5/7; 6/8

SDRAM RAS-to-CAS Delay
2/ 3 Set a delay between the assertion of RAS and CAS.

SDRAM RAS Precharge Time
2/3 Default setting is recommended.

System BIOS Cacheable
Besides conventional memory, the system BIOS area is also cacheable.

Video BIOS Cacheable
Besides conventional memory, video RAM area is also cacheable.

Memory hole at 15M-16M
Enabled Memory hole at 15-16M is reserved for expanded ISA card.

Delayed Transaction
The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select *Enabled* to support compliance with PCI Specification version 2.1. The default setting is Disabled.

AGP Graphics Aperture Size (MB)
The field sets aperture size of the graphics. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without any translation. The options available are 4M, 8M, 16M, 32M, 64M, 128M and 256M. The default setting is 64M.

System Memory Frequency
Options: Auto, 100MHz, 133MHz.

5.5 Integrated Peripherals

CMOS Setup Utility – Copyright (C) 1984 – 2001 Award Software Integrated Peripherals		
On–Chip Primary PCI IDE	Enabled	Item Help
On–Chip Secondary PCI IDE	Enabled	
IDE Primary Master PIO	Auto	
IDE Primary Slave PIO	Auto	Menu Level ►
IDE Secondary Master PIO	Auto	
IDE Secondary Slave PIO	Auto	
IDE Primary Master UDMA	Auto	
IDE Primary Slave UDMA	Auto	
IDE Secondary Master UDMA	Auto	
IDE Secondary Slave UDMA	Auto	
USB Controller	Enabled	
USB Keyboard Support	Disabled	
Init Display First	PCI Slot	
IDE HDD Block Mode	Enabled	
Onboard FDC Controller	Enabled	
Onboard Serial Port 1	[3F8/IRQ4]	
Onboard Serial Port 2	[2F8/IRQ3]	
UART Mode Select	[Normal]	
RxD, TxD Active	[Hi, Lo]	
IR Transmission Delay	[Enalbed]	
UR2 Duplex Mode	[Half]	
Use IR Pins	[IR-Rx2Tx2]	
Onboard Parallel Port	[378/IRQ7]	
Parallel Port Mode	[SPP]	
EPP Mode Select	[EPP1.7]	
ECP Mode Use DMA	[3]	
Pwron After PWR-Fail	[Former-sts]	
Watch Dog Timer Select	[By AP]	
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10: Save ESC: Exit F1:General Help F5: Previous Values F6: Fail - Save Defaults F7: Optimized Defaults		

On-Chip Primary Secondary PCI IDE
Enables or disables On-Chip Primary/Secondary PCI IDE.

IDE Primary/Secondary Master/Slave PIO
Mode 0 – 4/ Auto: Defines the IDE primary/secondary master/slave mode.

IDE Primary/Secondary Master/Slave UDMA

Auto/ Disabled: Ultra DMA mode will be enabled if an Ultra DMA device is detected.

USB Controller
Enables or disables onchip USB controller.

USB Keyboard Support
Enabled will support USB Keyboard under DOS status.

Init Display First
PCI Slot Initializes the PCI VGA first. Onboard Initializes the onboard VGA first. For PCI VGA or onboard VGA, the one initialized first functions.

IDE HDD Block Mode
Allows IDE HDD to read/write several sectors at each time. IDE HDD only reads/writes one sector at each time.

Onboard FDC Controller
Enables or disables onboard FDC.

Onboard Serial Port 1/2
3F8/IRQ4,2F8/IRQ3.3E8/IRQ4,2E8/IRQ3. Defines the onboard serial port address and required interrupt number. *Auto* Onboard serial port address and IRQ are automatically assigned. Disabled: Onboard serial port is disabled.

UART Mode Select
Normal. Select the UART Mode.

RxD, TxD Active
Hi, Lo/ Lo, Hi/ Lo, Lo/ Hi, Hi

IR Transmission Delay
Enabled/ Disabled

UR2 Duplex Mode
Half/ Full

Use IR Pins
IR-Rx2Tx2/ RxD2, TxD2

Onboard Parallel Port
378/IRQ7, 278/IRQ5, 3BC/IRQ7. Defines onboard parallel port address and IRQ channel. Disabled Onboard parallel port is disabled.

Parallel Port Mode
SPP/ EPP/ ECP/ ECP+EPP Defines the parallel port mode.

EPP Mode Select
EPP1.7/ EPP1.9

ECP Mode Use DMA
3/ 1

Pwron After PWR-Fail
System will stay off or power on after a power interrupt. Options:
OFF (default): System always stays off after a power interrupting.
Former-sts: Stay off or power on depends on system safe shut-down or power fail.
ON: Systems always powers on after a power interrupt.

Watch Dog Timer Select: By AP
This Watch Dog Timer in supper I/O chip can be enabled/programmed by applications.

5.6 Power Management Setup

CMOS Setup Utility – Copyright (C) 1984 – 2001 Award Software Power Management Setup		
Power Supply Type	[AT]	Item Help
Power Management	[User Define]	
Video Off Method	[DPMS]	
Video Off In Suspend	[YES]	Menu Level ►
Suspend Type	[Stop Grant]	
MODEM Use IRQ	[NA]	
Suspend Mode	[Disabled]	
HDD Power Down	[Disabled]	
Soft – Off by PWR – BTTN	[Instant–Off]	
Resume by ring	[Disabled]	
CPU Thermal – Throttling	[50.0%]	
Resume by Alarm	[Disabled]	
* Date (of Month) Alarm	0	
* Time (hh:mm:ss) Alarm	0 0 0	
** Reload Global Timer Events **		
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10: Save ESC: Exit F1:General Help F5: Previous Values F6: Fail - Save Defaults F7: Optimized Defaults		

Power Supply Type
Select the type of power supply. AT, ATX.

Power Management
Disabled: Global Power Management (PM) will be disabled.
User Define: Users can configure their own Power Management Timer.
Min Saving Pre - defined timer values are used. All timers are in their MAX values.
Max Saving Pre - defined timer values are used. All timers are in their MIN values.

Video Off Method
Blank Screen: The system BIOS will only blank off the screen when disabling video.
V/H SYNC+Blank: In addition to Blank Screen, BIOS will also turn off the V-SYNC & H - SYNC signals from VGA card to monitor.
DPMS: This function is enabled only for VGA cards supporting DPMS.
Note: When the green monitor does not detect the V/H-SYNC signals, the electron gun will be turned off.

Video Off In Suspend
Choose Yes to disable video when entering suspend mode.

Suspend Type
Stop Grant, PwrOn Suspend. Selects the Suspend type.

MODEM Use IRQ
3, 4, 5, 7, 9, 10, 11, NA. Special wake-up event for Modem.

Suspend Mode
Disabled: The system never enters Suspend mode by timer.
1 Min ~ 1Hr: Defines the continuous idle time before the system enters Suspend mode. If any items defined in "PM Events" are on and activated, the system will be woken up.

HDD Power Down
Disabled: HDD's motor will not be off by timer.
1 - 15 Min: Defines the continuous HDD idle time before the HDD enters power saving mode (motor off).

Soft-Off by PWR-BTTN
This item only display when you choose "ATX" in "Power Supply Type".
Instant-Off: The system will immediately power off once the power button is pressed.
Delay 4 sec: The system will power off when power button is pressed for 4 seconds.

Wake-Up by PCI Card
Enabled Allows the system to be waken up by PCI card.

CPU Thermal Throttling
12.5%, 25%, 37.5%,50%, 62.5%, 75%, 87.5%. Selects the duty cycle of the STPCLK# signal, and slowing down the CPU speed when the system enters green mode.

Resume by Alarm
Enabled RTC alarm can be used to generate a wake-up event to power up the system.
Disabled RTC has no alarm function.

Reload Global Timer Events
Enabled reload global timer when following event occur.
Primary/Secondary IDE 0/1
FDD, COM. LPT Port
PCI IRQ [A-D] #

5.7 PNP/PCI Configuration Setup

CMOS Setup Utility – Copyright (C) 1984- 2001 Award Software PnP/PCI Configuration		
Reset Configuration Data	[Disabled]	Item Help
Resources Controlled By	[Auto <ESCD>]	
* IRQ Resource	[Press Enter]	Menu Level ►
* DMA Resource	[Press Enter]	
* Memory Resource	[Press Enter]	
PCI/VGA Palette Snoop	[Disabled]	
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10: Save ESC: Exit F1:General Help F5: Previous Values F6: Fail - Save Defaults F7: Optimized Defaults		

Reset Configuration Data
Default setting is Disabled. Select Enabled to reset ESCD when you exit Setup, if you have installed a new add-on and the system reconfiguration has caused serious conflicts preventing the OS from booting.

Resources Controlled By (IRQ/DMA/Memory Resource)
Auto(ESCD)/ Manual. BIOS can automatically configure all boot and PnP compatible devices. If you choose Auto, you cannot select IRQ DMA and memory base address fields, because BIOS automatically assigns them.

PCI/VGA Palette Snoop
Disabled is default setting. Enabled Non-standard VGA cards such as graphics accelerators or MPEG video cars may not show colors properly. Enabling this item can solve this problem.

5.8 PC Health Status

CMOS Setup Utility – Copyright (C) 1984- 2001 Award Software PC Health Status	
CPU Warning Temperature [Disabled] Current System Temp. Current CPU Temperature Current CPU FAN Speed CPU Vcore (V) VTT (V) Vcc 3.3 (V) +5 V +12 V RTC Battery Voltage Standby Power Supply	Item Help Menu Level ►
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10: Save ESC: Exit F1:General Help F5: Previous Values F6: Fail - Save Defaults F7: Optimized Defaults	

CPU Warning Temperature
An alarm will beep when the CPU temperature is over this value. Disabled No alarm beep.

Current System/CPU Temp
The temperature of the system or CPU.

Current CPU FAN Speed
The speed of the CPU FAN(rpm).

5.9 Frequency/Voltage Control

CMOS Setup Utility – Copyright (C) 1984- 2000 Award Software Frequency/Voltage Control		
Auto Detect DIMM/PCI Clk	[Enabled]	Item Help
Spread Spectrum	[Disabled]	
CPU HOST/PCI Clock/PC133	[Default]	Menu Level ►
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10: Save ESC: Exit F1:General Help F5: Previous Values F6: Fail - Save Defaults F7: Optimized Defaults		

Auto detect DIMM/PCI Clk
Enabled to shut off the clock of empty DIMM or PCI slot(s) to reduce EMI. Disabled does not shut off the clocks.
Warning: Be sure your selection is right. CPU over speed will be dangerous!

Spread spectrum
Set the bus frequency/Spread Spectrum/PC133 Spec

CPU Host/PCI Clock/PC133 Default
This item's options will change automatically based on CPU FSB.

5.10 Load Defaults

Load Optimized Defaults
The Optimized Defaults are common and efficient. It is recommended to load the optimized defaults at first, and then modify the needed configuration settings. Select this item and press <Enter>, the following message will display, type in "Y" to load the default values, type "N" to cancel.

Load Fail-Safe Defaults
The safest default settings. You can use this function to detect the errors. Select this item and press <Enter>, the following message will display, type in "Y" to load the default values, type "N" to cancel.

5.11 Password Setting

When you select "USER PASSWORD" or "SUPERVISOR PASSWORD" and press <Enter>, the following message will appear at the center of the screen:

Input the password, up to eight characters, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection.

To disable password, just press <Enter> when you are prompted to enter password. A message as below will confirm the password being disabled. Once the password is disabled, the system will boot and you can enter BIOS Setup freely.

If you have selected **"System**" in "Security Option" of "BIOS Features Setup" menu, you will be prompted for the password every time the system reboots or any time you try to enter BIOS Setup.
If you have selected **"Setup**" at "Security Option" from "BIOS Features Setup" menu, you will be prompted for the password only when you enter BIOS Setup.

Supervisor Password has higher priority than User Password. You can use Supervisor Password when booting the system or entering BIOS Setup to modify all settings. Also you can use User Password when booting the system or entering BIOS Setup but can not modify any setting if Supervisor Password is enabled.

5.12 Exit BIOS Setup

After you have finished the configuration of BIOS, save your settings and exit setup utility. Select "Save & Exit Setup" and press <Enter>, the following message will display, type "Y" and press <Enter> to confirm.

If you do not want to save the settings, select "Exit Without Saving " to exit setup utility without saving any change.

CHAPTER 6 DRIVER INSTALLATION

The Drivers CD is an AutoRun CD. When you put it into the tray of CD-ROM drive, it will be executed automatically and the "Motherboard Drivers and Utilities Installation" wizard will appear after a while. If it cannot be executed automatically, please double click the "AUTORUN.EXE" in the root directory of CD-ROM.

The related information will list at the right field, such as drivers, utilities, manuals and catalog etc. Click "Browse this CD" button to see the detail contents, or click " Exit to Windows" to exit this wizard.

Following drivers must be installed for FSB-1611:

Intel Chipset Software Installation Utility
Intel 815E VGA Drivers
Intel 82559ER LAN Drivers

Please select the driver according to your operation system, and click "Go!" to install.

Other drivers and utilities are optional only and depend on your requirements.

CHAPTER 7 WATCHDOG CONFIGURATION

7.1 Watchdog Timer Application Interface

The watchdog is a timer designed to reset the CPU or generate an interrupt if the system comes to a standstill for any unknown reason. This is useful in applications where the CPU card will be used in an unmanned or standalone situation.

The FSB-1611 has a build-in watchdog timer. The super I/O chip, WINBOND® W83627HF, implements it.

The watchdog timer contains a 1-second/minute resolution down counter. The down counter can be programmed within the range from 1 to 255 seconds/minutes. Writing any new non-zero value to the down counter will cause the watchdog timer to reload and start to count down the new value. As the counter reaches zero, the system will be reset or an interrupt generated, which is determined by the time-out event configuration.

7.2 Configuring the watchdog timer

The system accesses the super I/O chip through Intel® LPC (Low Pin Count) interface. A fixed I/O ranged 2E~2Fh supports index access for super I/O configures.

The I/O chip, W83627HF uses compatible PnP protocol to access configuration registers for setting up variable configurations. In W83627HF, there are eleven logic devices. Each logic device has its own configuration registers (above CR30). Host can access those registers by writing an appropriate logic device number into device select register CR7. Watchdog timer shares the same logic number 8 with GPIO port 2.

To program watchdog timer or other W83627HF configuration registers, the following configuration sequence must be followed:

(1) Enter the extended function mode

To place the chip into the extended function mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 0x2E).

The following example is encoded with Turbo C 2.0. Symbol `Superio_Config_Port` *is the address of EFER and must be predefined as a constant 0x2E.*

```
/*****************************************************
 *     Enter Logic Device Program Mode
 *****************************************************/
```

```
int Superio_Enter_Config(void)
{
       outp(Superio_Config_Port, 0x87);
       outp(Superio_Config_Port, 0x87);
       return 0;
}
```

(2) Configure the configuration registers

The chip selects the logical device and activates the desired logical devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). EFIR is located at the same address as EFER (0x2E), and EFDR is located at address (EFIR+1).

```
#define NEWIODELAY() asm OUT 0EBh,AL   /* delay for I/O access */

int Superio_Set_Reg(int RegInx,    int RegVal)
{
       outp(Superio_Config_Port, RegInx);
       NEWIODELAY();
       outp(Superio_Config_Port+1, RegVal);
       NEWIODELAY();
       return 0;
}

int Superio_Get_Reg(int RegInx)
{
       int    RegVal;
    outp(Superio_Config_Port, RegInx);
    NEWIODELAY();
    RegVal = inp(Superio_Config_Port+1);
    NEWIODELAY();
    return    RegVal;
}
```

First, write the device select register number (0x07) to the EFIR and then write the number of the desired logical device (0x08 for watchdog timer/GPIO port 2) to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Invoking following routine performs a logic device selection for watchdog. The entry parameter `LgcDevNum` is predefined as 0x8.

```
int Set_Logic_Device(int LgcDevNum)
{
   Superio_Set_Reg(0x7, LgcDevNum);  /* LgcDevNum=8 for watchdog */
   return     0;
}
```

Secondly, write the address of the desired configuration register within the logical device to the EFIR and then write (or read) the desired configuration register through EFDR.

The detail of watchdog configuration register programming will be described in the next paragraph.

(3) Exit the extended function mode.

To exit the extended function mode, one write of 0xAA to EFER is required. Once the chip exits the extended function mode, it is in the normal running mode and is ready to enter the configuration mode.

```
/*****************************************************
 *     Exit Logic Device Program Mode
 *****************************************************/
int Superio_Exit_Config(void)
{
       outp(Superio_Config_Port, 0xaa);
       return 0;
}
```

7.3 The detail of watchdog programming

The Watchdog timer output pin, WDTO shares the same physical pin with GPIO24. The status of GPIO24 configuration registers must be programmed to a known value whatever the application configures the watchdog time-out event as system reset or interrupt.

(1) Configure watchdog time-out event

The watchdog can be configured as system reset output or generate an interrupt if the system comes to a standstill for any unknown reason. If it is set as system interrupt, the following lines, predefinitions must be implemented.

```
#defineWDTIRQMod
/* Select time-out event IRQ number (0 to 15, 2 for SMI) */
#defineIRQSource 5/*eg. Select Watchdog interrupt connect to IRQ5*/
```

The counter resolution of the watchdog timer should be predefined too. `WDTCntMod=0` is for 1-sec resolution and 1 for 1-min resolution.

```
#defineWDTCntMod     0      /* 0 -- 1-second resolution */
                          /* 1 -- 1-minute resolution */
```

The following is an example to initialize the watchdog.

```
int ConfigWDT(void)
{
    int       iRetVal;

    /* Enter super I/O chip configuration mode */
    Superio_Enter_Config();

    /* Select logic device 8, watchdog to configure */
    Set_Logic_Device(0x8);

    /* Configure GPIO24 as output pin */
    iRetVal = Superio_Get_Reg(0xf0);
    iRetVal &= ~0x10;       /* clear bit4, GPIO24 as output */
    Superio_Set_Reg(0xf0, iRetVal);
```

```
    /* Configure GPIO24 output LOW level */
    iRetVal = Superio_Get_Reg(0xf1);
    iRetVal &= ~0x10;       /* clear bit4, GPIO24 output 0 */
    Superio_Set_Reg(0xf1, iRetVal);

    /* Configure GPIO24 output non-inversion */
    iRetVal = Superio_Get_Reg(0xf2);
    iRetVal &= ~0x10;       /* clear bit4, GPIO24 non-inversion */
    Superio_Set_Reg(0xf2, iRetVal);
#ifdef WDTIRQMod

   /* Select GPIO/WDTO pin as GPIO */
   iRetVal = Superio_Get_Reg(0x2b);
   iRetVal |= 0x10;     /* Set bit4,Select GPIO/WDTO pin as GPIO */
   Superio_Set_Reg(0x2b, iRetVal);

   /* Note: Application should provide an interrupt service */
   /* Select time-out event IRQ number (0 to 15, 2 for SMI) */
   Superio_Set_Reg(0xf7, IRQSource);

#else

   /* Select GPIO/WDTO pin as WDTO */
   iRetVal = Superio_Get_Reg(0x2b);
   iRetVal &= ~0x10; /* Clear bit4, Select GPIO/WDTO pin as WDTO */
   Superio_Set_Reg(0x2b, iRetVal);

#endif

   /* Select watchdog timer count mode (sec/min) */
   iRetVal = Superio_Get_Reg(0xf5);
   iRetVal &= ~0x8;          /* Count mode config bit */
   if (WDTCntMod)
      iRetVal |= 0x8;
   Superio_Set_Reg(0xf5, iRetVal);

   /* Set watchdog time-out value, disabled */
   Superio_Set_Reg(0xf6, 0);

   /* Exit super I/O chip configuration mode */
   Superio_Exit_Config();

   return     0;
}
```

(2) Enable/Refresh the watchdog timer

The following codes show how to refresh the watchdog timer. It must be invoked at least once every cycle in application. The entry parameter `iTimOutVal` is ranged `0x1` to `0xff`. The watchdog timer should be initialized before it is enabled or refreshed.

```
int RefWDT(int iTimOutVal)
```

```
{
    /* Enter super I/O chip configuration mode */
    Superio_Enter_Config();

    /* Select logic device 8 to configure */
    Set_Logic_Device(0x8);

    /* Set watchdog time-out value, disabled */
    Superio_Set_Reg(0xf6, iTimOutVal);

    /* Exit super I/O chip configuration mode */
    Superio_Exit_Config();

    return    0;
}
```

(3) Disable the watchdog timer

Invoke `RefWDT()` with parameter `iTimOutVal=0` will disable the watchdog timer.

```
RefWDT(0x0);
```

(4) How to check watchdog timer status

If the watchdog is configured as a system time-out reset. Bypass the section.
If the watchdog time-out event is configured as a system interrupt, the application program should handle the preset IRQ and provide an interrupt service routine. Following routine shows how to check if the generated interrupt is required from watchdog.

```
int ChkWdtIrq(void)
{
    int    iRetVal;

    /* Enter super I/O chip configuration mode */
    Superio_Enter_Config();

    /* Select logic device 8 to configure */
    Set_Logic_Device(0x8);

    /* Check watchdog timer status */
    iRetVal = Superio_Get_Reg(0xf7);
    iRetVal &= 0x10; /* Check bit4, 1 – Time-out event occurred */

    /* Exit super I/O chip configuration mode */
    Superio_Exit_Config();

       if     (iRetVal)
              return 1;     /* Watchdog time-out occurred */
    return    0;            /* Watchdog timer counting */
}
```